A Simulation Study on the Impact of Lithographic Process Variations on CMOS Device Performance

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ABSTRACT

In this paper, we demonstrate how a direct coupling of a lithography simulation program and a semiconductor device simulation tool can be used to investigate the impact of lithographic process variations on nano-scaled CMOS devices. In contrast to conventional evaluation criteria such as process windows, mask error enhancement factor (MEEF), or CD (critical dimension) uniformity, the lithography process is regarded in a more holistic fashion as a means to an end. As a consequence, the ultimate figure of merit is determined by the performance of the device.

Lithography simulations are conducted using a rigorous EMF solver for the computation of the mask nearfield. TCAD process and device simulations are performed for an ultra thinned body fully depleted silicon on insulator (UTB FD-SOI) nMOSFET, with a physical gate length of 32 nm. Electrical parameters such as on- and off-current, threshold voltage, sub-threshold slope, gate-capacitance, and contact resistances are computed and extracted. The impact of lithographic process variations on the electrical behavior of the target device is surveyed and illustrated. Moreover, we present an adjusted lithography process window defined by the electrical behavior of the device.

In addition to a discussion of the obtained results, this paper also focuses on the software design aspects of interfacing a lithography simulation environment with a device simulator. The steps involved in extracting parameters and transferring them from one program to the other are explained, and further automation capabilities are suggested. Moreover, it is illustrated how this approach can be extended towards an integrated litho/device process optimization procedure.

Keywords: Lithography Simulation, Process Simulation, Device Simulation, Process Variations

1. INTRODUCTION

In the past years, increasing attention has been paid to the impact of lithography process steps on the manufacturability and yield of chips. Long gone are the days when OPC (optical proximity correction) was solely in the domain of lithographers. Today, it has become part of the chip designer's everyday business. Just as litho-friendly design and lithography hot-spot detection are a matter of course for modern DfM (desing for manufacturability) or DfY (design for yield). Still, the gap between lithography and chip design has not yet been bridged as well as it seems. OPC is still mostly rule-based and not a result of straight-forward optimizations. Rigorous electromagnetic field (EMF) simulations, that are inevitable to predict the effects of sub-wavelength imaging, are still not realizable on full-chip level. Moreover, so far very few attempts have been made to investigate the impact of lithography on the electrical parameters of the device.[1,2] Related studies aim at the influence of LER (line edge roughness),[3,4] on litho-induced variations on the circuit behavior,[5–7] or on design issues.[8–11]

Due to the aggressive scaling of CMOS devices in the last decade, the impact of process-induced variations on the electrical behavior of CMOS devices has become an issue of increasing relevance. Especially the influence of what is said to be random variations, that can even be observed in devices of the same chip, is far from negligible. These on-chip variations may, for example, lead to critical path failures in circuit units. That is, the usable time to process data in a certain clock period is insufficient for this path, rendering the entire chip unemployable. It is well know that lithography is one of the chief causes for on-chip variations.

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As comprehensive experimental investigations on the direct influence of lithography process variations on the electrical behavior are virtually impossible, TCAD and compact model simulations (e.g. SPICE) offer a viable alternative. Especially in the regime of recent CMOS device architectures such as silicon on insulator (SOI) transistors, rigorous, process-aware TCAD simulations are indispensable as they account for a multitude of effects not captured by compact models. In order to allow for a realistic and broad study on litho-driven effects on state-of-the-art CMOS transistors, all device simulations in this work have been performed using a full TCAD model.

As a drawback, however, TCAD simulations tend to be very time-consuming, especially when performed in conjunction with process simulation steps. Thus, to be able to carry out a variation study, individual simulations have to be computed in parallel, requiring an automatic distribution strategy.

In this paper, we present a holistic simulation approach. Instead of regarding lithography, process, and device simulation steps as sealed-off entities, we propose to regard the results of the entire flow as evaluation criteria for lithography. Thus, lithography parameters are directly related to electrical parameters of a silicon on insulator MOSFET not only for impact investigations but also for lithography process window optimization.

2. SIMULATION FRAMEWORK

The variation study proposed in this work requires an environment that allows for a coupled simulation of lithography, process, and device simulations. The goal is to provide an easy-to-use tool that can be used not only for this investigation but also for future design-of-experiment (DOE) and full blown optimization tasks. The number of simulations and the computation times in the regime of rigorous TCAD process and device simulations require this framework to possess an automated distribution procedure such that several simulations can be performed in parallel. For the purpose of this work, we have utilized the distribution environment DisPyTE[12] that has been previously introduced for distributed heuristic optimization tasks. The framework is implemented in the scripting language Python and makes use of the Python network toolkit Twisted.[13] In contrast to conventional network communication strategies—such as MPI (message passing interface)—Twisted provides an "event-driven" interface, a technique also used in graphical user interface toolkits: Instead of a sequential processing of tasks, a controlling unit remains in a loop and waits for events, that may for example be triggered by mouse clicks or, in the case Twisted, by network events.

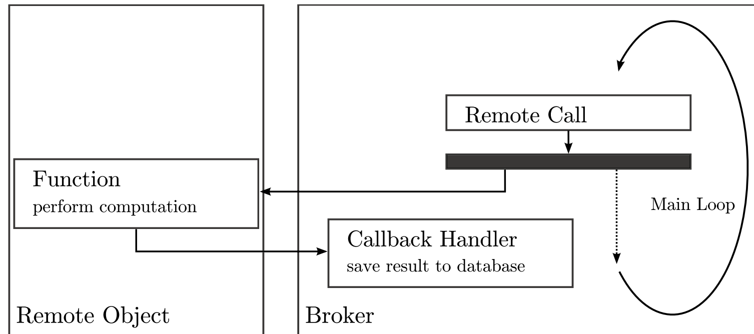


Figure 1. Event-driven network interaction: A broker distributes a time-consuming computation to a remote object. The processing of the result is done by a callback handler. Hence, the broker does not block but is ready to request further services.

Figure 1 demonstrate the principal of event-driven programming with Twisted. A controlling unit (*broker*) requests a service from a remote object. This object may reside in another process, possibly on a different machine than the broker. The broker does not wait for the remote function to return its result. Instead it remains in the main loop and can hence request further services, for example, on other machines. A callback handler is installed and waits for the remote function to return its result. Once the result is obtained, the callback handler can further process it. In the simple example in Figure 1 the task is to perform a time-consuming computation.

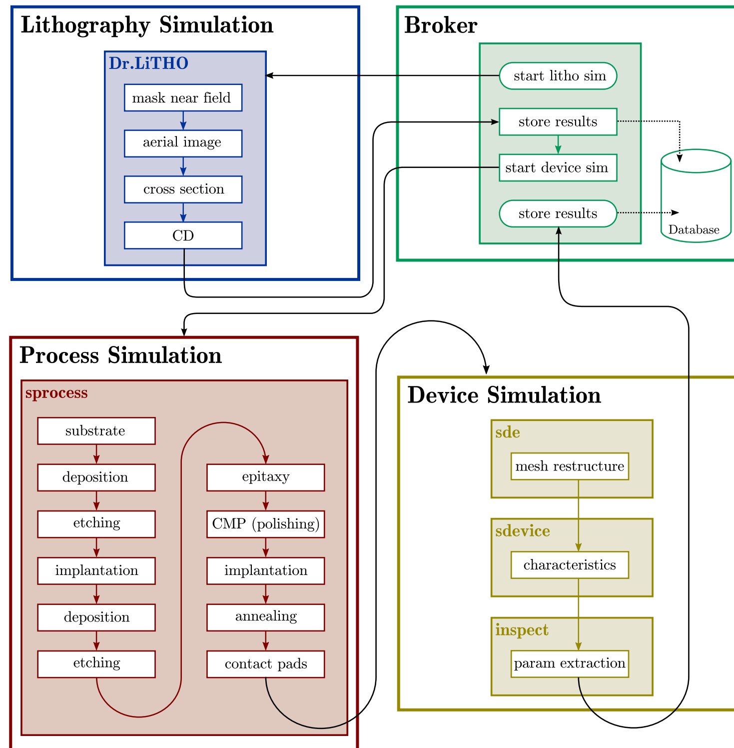


Figure 2. Simulation flow. The controlling unit (broker; upper right) distributes simulation tasks to different workers. First, a lithography simulation step (upper left) is deployed. Results are caught by the broker and stored in a database. Next, the process simulation (lower left) is performed with the previously computed litho results. Finally, after the device simulation (lower right) is finished, the extracted results are passed back to the broker and stored.

The callback handler's only task is to store the result into a database. Instead of requesting a single service on only one machine, the broker could as well send jobs to different "workers."

In this work, the broker manages the parameter variations, whereas the workers provide the simulation services. In order to allow for a high degree of flexibility, we have utilized the OptProb interface[14] that has already been used in the scope of optimization tasks. OptProb not only provides methods for defining parameters and figures of merit but also an easy-to-use link-up to different optimization routines. Although in this work an elementary parameter variation is performed, future extensions, utilizing design-of-experiments or optimization setups, can be integrated in a straight-forward manner.

The general flow of the simulation framework is depicted in Figure 2. After the controlling unit, the broker, and a desired number of workers have been started, parameter sets are generated and passed to the workers. In a first step, the lithography simulation is performed. The simulation environment used in this work is *Dr.LiTHO*, the Fraunhofer IISB lithography simulation environment.[15] Since the *Dr.LiTHO* framework uses Python as a front-end language, parameters can be directly passed to it. Once the lithography simulation step is finished, a callback in the broker is triggered, which handles the storage of the results to a database. The so obtained intermediate litho results are passed to the next simulation step, the process simulation. In the current version, this is solely the CD, that is extracted from the cross section of the aerial image and decremented by an etch bias of 13 nm. Process and device simulations are performed using the *Sentaurus* suite by Synopsys.[16] The *Sentaurus* simulators and tools can be controlled and configured using so-called command files. Instead of directly calling *Sentaurus* programs, a simple wrapper has been implemented in Python. This wrapper serves as a worker for the simulation environment—that is, it is remotely callable and can be fed with parameters from previous simulation steps. Upon a remote call with current parameters, the wrapper generates command files with these parameters and executes the *Sentaurus* process simulator (*sprocess*). In a next step, a mesh refinement, that accounts for the

altered gate length, is performed—using the *Sentaurus* structure editor. The device simulation step is carried out with *sdevice*. The results of this device simulation step are extracted with *inspect* and so exposed to the worker, from which all simulations are called. Finally, the worker returns these results to the callback routine of the broker, which stores them in the database; currently supported are MySQL, PostgresSQL, and sqlite, which allows the use of a simple database file. Evaluation procedures can simply access the database and hence perform an efficient data mining.

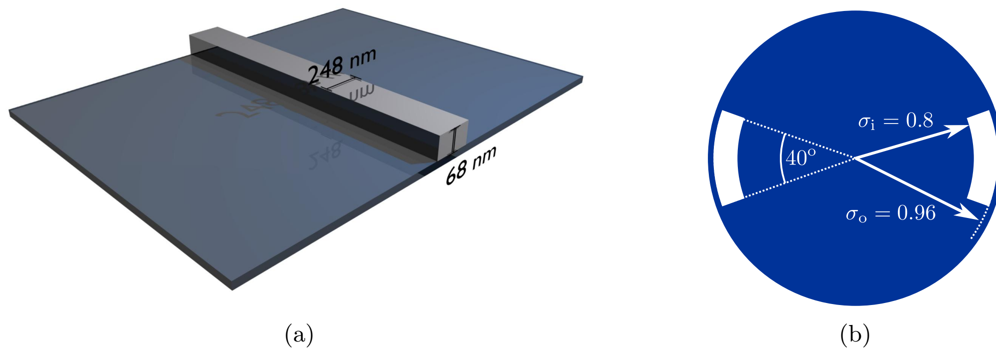
The proposed distribution framework is platform independent. Thus, it can also be used in heterogeneous networks—provided, of course, the utilized simulators are available on the corresponding architecture. In addition, it provides a certain level of fault tolerance in that computations on non-responding workers are re-distributed. Moreover, the framework may be employed in dedicated HPC (high performance computing) systems in which it can be operated with virtually any scheduler.

3. SIMULATION SETTINGS

In this section, the settings for the individual simulation steps are briefly discussed. The first sub-section presents the reticle and optical system parameters for the lithography simulation. Additionally, the applied models are briefly discussed. In the second sub-section, the steps involved in the process simulation and device simulation settings are shown.

3.1 Lithography Simulation

This work aims at the variation of lithography process conditions and the impact of the resulted gate lengths on the electrical behavior of the transistor. Thus, a 193 nm wavelength water immersion lithography process for the simulation of an isolated line was set up. The NA is 1.2.



(a) (b)

Figure 3. Lithography settings: (a) Quasar dipole illumination. Inner radius (σ_i): 0.8; outer radius (σ_o): 0.96; opening angle: 40°. (b) Reticle layout. MoSi absorber on glass substrate, dimensions are in reticle scale.

Figure 3(a) shows the reticle, an AttPSM (attenuated phase shifting mask) with a MoSi absorber (n: 2.442; k: -0.586) on a glass substrate. After a coarse pre-optimization of the process window, the absorber width was set to 62 nm (wafer scale), a thickness of 68 nm (reticle scale) was chosen. As in the regime of sub-wavelength imaging EMF effects have to be taken into account, in this work, all mask nearfield computations are performed with the Waveguide Method of *Dr.LiTHO* and without Hopkins approximation.

As illumination source, we use a dipole quasar setup with an inner radius (σ_i) of 0.8 and an outer radius (σ_o) of 0.96 (normalized to NA). The opening angles of the poles is 40° (see Figure 3(b)). The light is y-polarized, with an IPS (intensity of preferred state) of 1. For this first study, no full photoresist model is applied. Instead a threshold model is used.

Figure 4 depicts the feasible process range that is obtainable with the specified process—as usual, a 10 % CD variation was permitted. Since no full resist model is applied, the threshold is assumed to indirectly render the

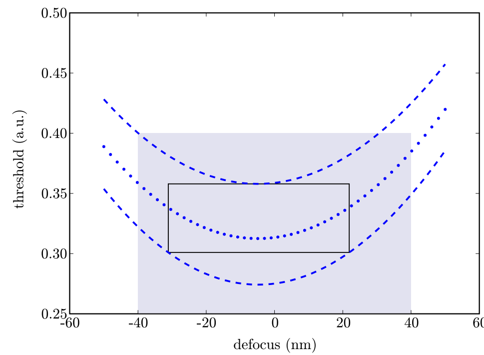


Figure 4. Lithography process window. Depth of focus: 52 nm, “threshold latitude”: 0.057. The grayish rectangle symbolizes the variation range.

exposure dose. A rectangular process window is used to demonstrate the region of a stable process. The focus shift and small asymmetries of the process window result from mask diffraction effects. Rigorous electromagnetic field simulation of the light diffraction from the masks reveals small phase shifts between the diffraction orders. The impact of these phase shifts on the process window is similar to that of optical wave aberrations of the projector lens such as defocus and spherical aberration.

Using the rectangular approximation of the process window, the depth of focus is 52 nm, yielding a “threshold latitude” of about $\pm 8.5\,\%$. The relatively small depth of focus is due to the fact that no assist features are applied. In order to study the impact of litho variations not only within feasible process conditions, the following variation range is chosen: defocus: [-40 nm, 40 nm], threshold: [0.25, 0.405]. The grayish highlighted rectangle in Figure 4 illustrates this region.

3.2 Process and Device Simulation

As a destination device for the variation study, a modern CMOS transistor, an ultra thinned body fully depleted silicon on insulator (UTB FD-SOI) nMOSFET, is selected. The target of the physical gate length is 32 nm, with a silicon body thickness (t_{Si}) of 10 nm, a gate oxide thickness (t_{ox}) of 1.2 nm, and a buried oxide (BOX) thickness (t_{BOX}) of 20 nm. The device is modeled using a full TCAD approach. The employed process simulator is *Sentaurus Process*, using its standard models. The channel of the transistor is lightly boron-doped with a doping concentration of $10^{15}\,\mathrm{cm}^{-3}$.

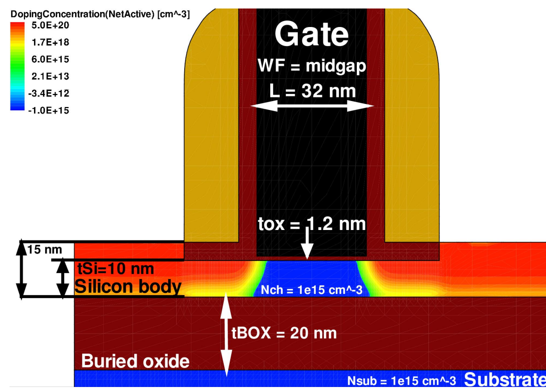


Figure 5. Geometrical shape of the fully depleted SOI based NMOS transistor and doping distribution

For the extensions, we simulate the implantation of arsenic with a dose of $10^{15}\,\mathrm{cm}^{-2}$ and an implantation energy of 2.0 keV. After the elevation of the source/drain regions by 5 nm, we model a second implantation step

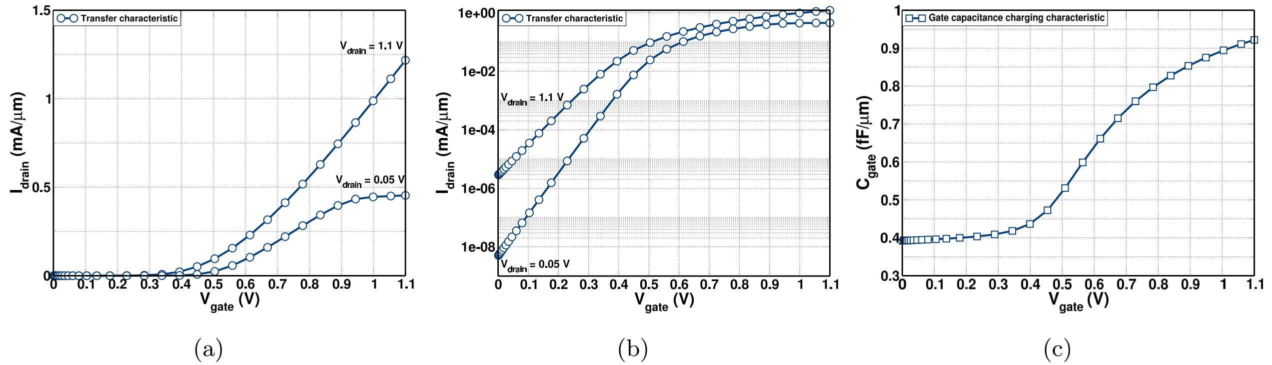


Figure 6. Performance of default device: (a) transfer characteristic with linear and (b) logarithmic scaling; (c) gate capacitance charging characteristic.

with the same dose and implantation energy as for the extensions. After that, a rapid thermal annealing (RTA) step is performed with a temperature of 1200°C and an annealing time of one millisecond. Figure 5 displays the final structure of the UTB FD-SOI nMOSFET.

Following the process simulation, the numerical grid is refined in order to account for an altered gate length, resulting from the CD variations. The refined grid is then applied to the subsequent device simulation step, using *Sentaurus Device*. Withing the device simulation step, the transfer characteristics for both the high and low biased case of the device and the gate capacitance charging characteristic are computed. The mobility of the carriers is calculated after the doping dependency model of Masetti,[17] the Lombardi[18] model for surface scattering, and the carrier-carrier scattering model of Conwell and Weisskopf.[19] The high-field saturation is adapted from the Caughey-Thomas[20] model with an adjustment of the saturation velocity to $2.2{\cdot}10^7$ cm/s, as it has been proposed by Bude[21] for nano-scaled CMOS devices. For the simulation of quantum-mechanical depletion, the modified local density approximation[22] (MLDA) is used.

The transfer characteristics for high biased and low biased conditions are evaluated by DC analysis, while the charging behavior of the gate capacitance is computed by an AC small signal analysis. The characteristics are shown in Figure 6.

As a result of the device simulation, several electrical parameters of the device can be extracted. The default device, that is, without any physical gate length variation, exhibits the following properties: an on-current (I_{on}) of 1.198 mA/µm, an off-current (I_{off}) of 1.189 nA/µm, a threshold voltage (V_{th}) of 319 mV, a sub-threshold slope (SSlope) of 94.144 mV/dec, and an on-state value of the gate capacitance (C_{gate}) of 0.96 fF/µm. Furthermore, we obtain an on/off current relation (I_{on}/I_{off}) of 1007569.4 and a switching speed (t_p) of 0.887 ps.

4. RESULTS AND DISCUSSION

As indicated before, we have varied the defocus and the threshold in the lithography simulation steps within the range: [-40 nm, 40 nm] × [0.25, 0.405]. The threshold was varied using a fixed increment of 0.005 (≡ 32 threshold steps). For each threshold step, we have randomly generated 268 defocus variations, yielding a total of 8576 variations. We have performed the experiment for both a normal and a uniform defocus distribution. The average calculation time for a single simulation was 7 minutes on a single core of an AMD Opteron 275 two-processor dual core machine, of which the lithography simulation step took less than 5 seconds. The time for an entire run was about 3 days, using 15 processor cores on a dedicated Linux cluster.

In a first step, we have investigated the influence of the variations in physical gate length on the electrical properties of the device. Figure 7(a) show the relation of drive current and leakage current obtained with the simulated devices. When compared to the drive and leakage current of the nominal device for different gate work-functions (WF), one can observe a pronounced disagreement in the slope. A similar behavior can be noted when comparing the relationship between leakage current and the device delay ($C_{gate}V_{DD}/I_{on}$) of the varied devices

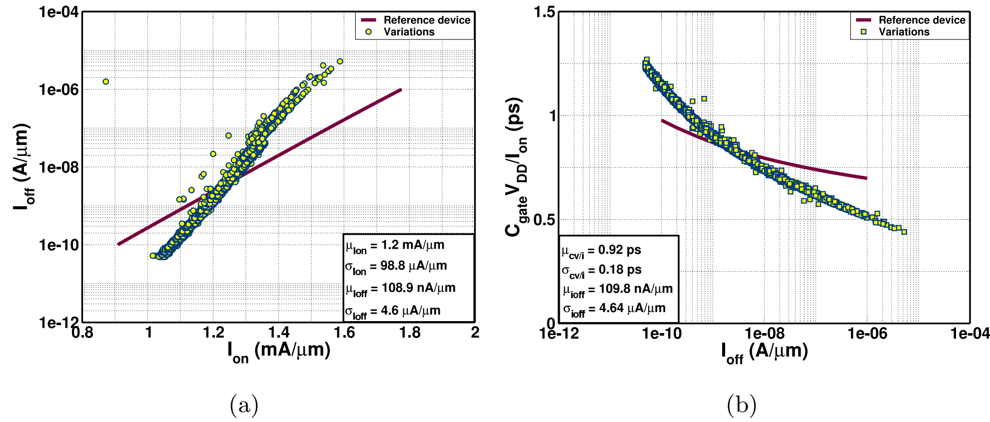


Figure 7. Comparison of generated variations with different work-functions on nominal device: (a) drive current against leakage current, (b) leakage current against switching speed

with WF-yielded values obtained for the nominal device (Figure 7(b)). Since the alteration of work-functions corresponds to a shift in the threshold voltage, the device delay cannot only attributed to the threshold voltage.

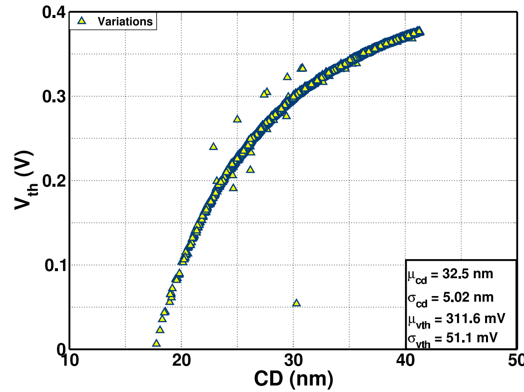


Figure 8. CD against threshold voltage.

Figure 8 illustrates the influence of the CD on the threshold voltage (V_{th}). The MOSFET shows a critical short channel behavior, that renders the device unemployable for CD values of about 17 nm and below, as it does not maintain an off-state.

The significant outlier at a CD value of about 32 nm might be caused by a mathematically correct yet non-physical solution of the device simulator. This may be attributed to the fact that with each variation, the mesh is refined, leading to changed conditions in subsequent simulation steps. Similarly, the remaining statistical blip may be originated by numerical imprecisions. This effect—that can of course also be observed in the following plots—will have to be investigated more closely in future work.

In a next step, we have investigated the sensitivity of the device to lithography process variations. For that purpose, we have extended the traditional Bossung Curves to plots that reveal the electrical behavior of the devices (Figure 9). Compared to the traditional Bossung Curves (Figure 9(a)), the sensitivity to defocus increases more significantly with higher exposure dose levels (lower thresholds). This effect is very pronounced for the threshold voltage and sub-threshold slope properties.

The difference between impact of dose (threshold) on CD or electrical parameters of the device can be demonstrated even more clearly by a direct plot, as done in Figure 10. There, the (de)focus is subdivided into three levels: -25 nm, best focus, 25 nm.

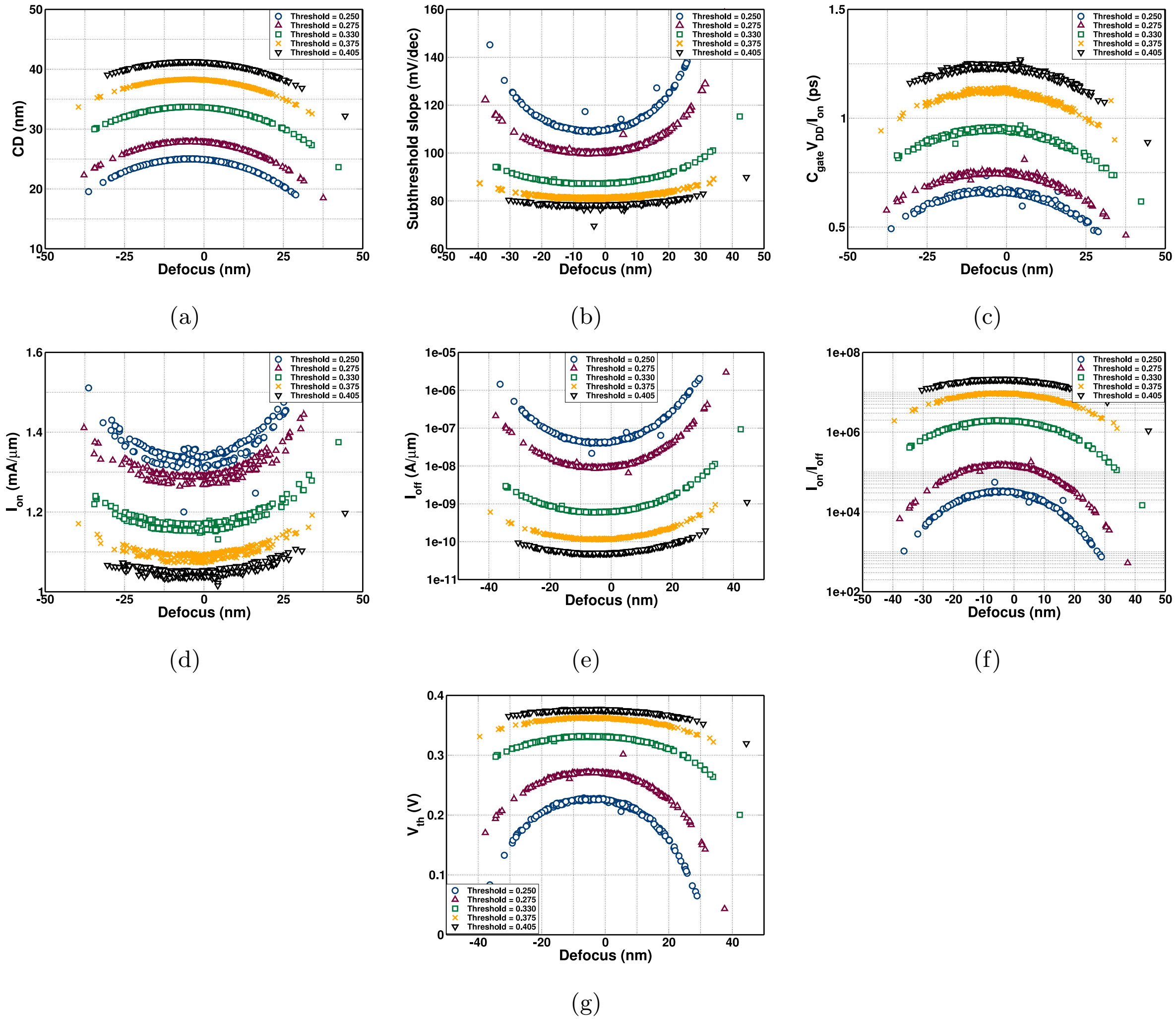


Figure 9. Extended Bossung Curves. Figure of merit in dependence of defocus for fixed dose (threshold) levels: (a) CD [traditional Bossung Curve], (b) sub-threshold slope, (c) device delay, (d) drive current, (e) leakage current, (f) I_{on}/I_{off} (g) threshold voltage

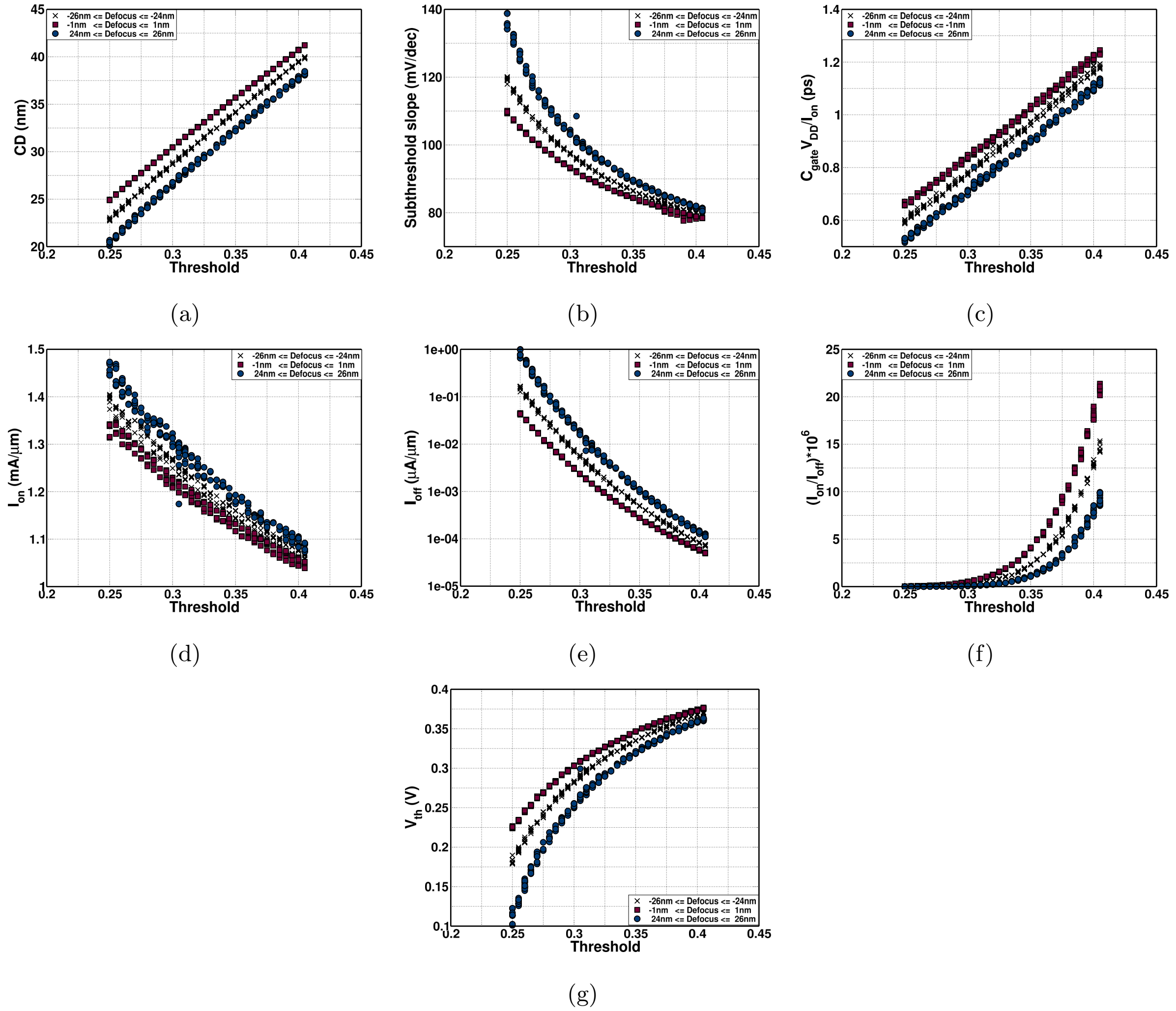


Figure 10. Figure of merit in dependence of threshold (exposure dose) for fixed focus values: (a) CD, (b) sub-threshold slope, (c) device delay, (d) drive current, (e) leakage current, (f) I_{on}/I_{off} (g) threshold voltage

For the lithography set-up presented in this work, the CD dependence on the threshold is strictly linear. Thus, the electrical device parameters exhibit the same behavior towards the threshold as they would towards a direct variation of the CD.

From the presented plots, one can expect that a merely CD-defined process window may still not guarantee the manufacturability of devices. Moreover, from the observations, one could deduce the constraints on dose and focus latitude. To be more systematic, one can also define a lithographic process window that guarantees for fluctuation of the electrical performance that tolerable for both device and circuit designers.

Figure 11 shows such a lithographic process windows in terms of device performance. The left figure (11(a)) shows the obtained variations of threshold against defocus. Different criteria, evaluating the device performance, are applied. The drive current is restricted to a range of ±10 % around 1.2 mA/µm (I_{on} criterion). Additionally, the gate-overdrive (GO) voltage (GO := V_{dd}-V_{th}) is to be in a ±5 % range of 581 mV (GO criterion). Finally, the sub-threshold slope (SSLope) should be smaller than or equal to 100 mV/dec (SSlope criterion). Each of these criteria confines the variation space. The resulted windows are indicated with dashed (Ion criterion), unevenly dashed (SSlope criterion), and solid lines (GO criterion). For the device investigated in this work, the GO criterion results in the narrowest window. It thus constitutes a first coarse, however feasible, approximation

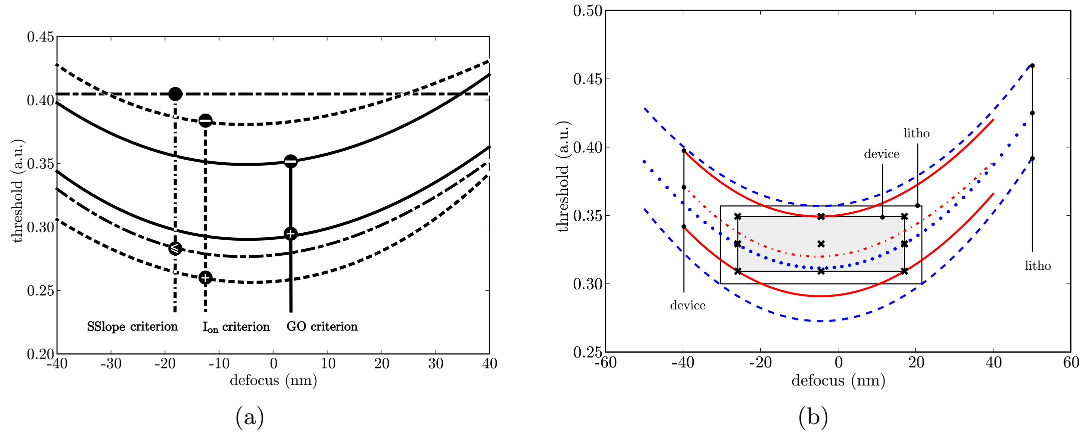


Figure 11. (a) Device evaluation criteria and resulted variation windows: the SSlope criterion confines the variation space to solutions with an SSlope of $\leq$ 100 mV/dec; the I_{on} criterion requires solutions to exhibit an I_{on} value of $\pm$10 % around 1.2 mA/μm; the GO criterion restricts the gate-overdrive to 581 mV with a tolerance of $\pm$5 %. (b) Process windows: The outer rectangle illustrates the region of a stable lithography process in terms of CD variation; the inner rectangle depicts a process window obtained by applying the device performance criteria as defined in (a).

of the tolerable fluctuation range. Variations resulted from etching and implantation steps are not taken into account.

The so obtained restricted sampling points can be used to define a process window that specifies a feasibility region for the lithographic process. This process region and the resulting process windows are illustrated in Figure 11(b). The outer rectangle illustrates the region of a stable process defined by the usual approach of allowing up to 10 % CD variations. The inner window is obtained by an evaluation of the performance of the specific device explored in this work. In the lithography case, the defocus latitude ranges from -30.4 nm to 21.61 nm. In the device case, it is within -25.88 nm and 17.11 nm. The threshold ranges are [0.3, 0.36] and [0.31, 0.35], respectively. The ratio of litho and device induced process windows strongly depends on the device. In the case of this work, the device process window is considerably smaller than the litho one. Different devices may of course lead to an increased process window. For the minimum, medial, and maximum defocus and threshold values in the device process window, CD values are show in Table 1.

Table 1. Lithography feature sizes for defocus and threshold settings obtained from device process window (cf. Figure 11.)

defocus (nm)	**threshold** 0.31	0.33	0.35
-25.88	CD: 42.61 nm	CD: 44.81 nm	CD: 46.97 nm
-4.38	CD: 44.55 nm	CD: 46.64 nm	CD: 48.70 nm
17.12	CD: 42.55 nm	CD: 44.75 nm	CD: 46.90 nm

Table 2 provides a summary and comparison of the results obtained from the purely CD-defined process window and that defined by the performance evaluations of the investigated device. Shown are the median, standard deviation, and the relative standard deviation for a normal and a uniform defocus distribution (italic type). By using the restricted litho process window, one can observe a significant reduction of the variations of the electrical parameters.

Table 2. Summary of device parameters. Mean values, standard deviations and relative standard deviations (RSD) for normally and *uniformly* (italic type) distributed defocus values, both for the lithography-defined and the device-defined process window (index d).

Parameter	μ	σ	RSD (%)	μ_d	σ_d	RSD_d(%)	default
CD (nm)	32.5	5.0	15.4	32.6	1.9	5.8	32.0
	31.1	*5.5*	*17.7*	*32.6*	*1.9*	*5.8*	
I_{on} (mA/μm)	1.19	0.096	8.1	1.18	0.038	3.2	1.198
	1.21	*0.11*	*9.1*	*1.18*	*0.037*	*3.14*	
I_{off} (nA/μm)	17.6	128.0	727.3	1.3	1.06	81.5	1.89
	83.3	*400.7*	*481.0*	*1.3*	*1.03*	*79.2*	
Vth (mV)	312.0	51.2	16.4	321.0	16.7	5.2	318.8
	293.0	*68.7*	*23.4*	*321.0*	*16.4*	*5.1*	
SSlope (mV/dec)	91.5	10.8	11.8	89.3	3.5	3.9	94.1
	95.6	*15.9*	*11.8*	*89.3*	*3.4*	*3.8*	
I_{on}/I_{off} ($\cdot 10^6$)	3.94	5.25	133.2	1.64	1.16	70.7	0.6
	150.9	*4.42*	*133.2*	*1.63*	*1.14*	*69.9*	
$C_{gate}V_{DD}/I_{on}$ (ps)	0.92	0.18	19.6	0.91	0.07	7.7	0.887
	0.87	*0.19*	*21.8*	*0.91*	*0.07*	*7.7*	

5. CONCLUSION

In this work we have presented a parameter variation study to investigate the impact of lithography variations on the electrical behavior of modern SOI transistors. For that, a simulation environment that allows for an easy integration of lithography, process, and device simulators has been implemented. The proposed framework incorporates a sophisticated distribution mechanism to be able to cope with the high number of evaluations and large computation times. Both a rigorous mask nearfield model and a full TCAD model, for process and device simulations, have been utilized to account for the large number of physical effects. Almost 9000 CD and thus MOSFET variations have been computed and analyzed.

We have proposed the extension of traditional Bossung Curves to illustrate the impact of the lithography process on the transistor properties. Furthermore, from the electrical parameters and an approximation of their tolerable ranges, we have computed a refined lithography process window. Within this process window, variations in the desired MOSFET could be reduced by a factor of two and more.

In the current version of the proposed simulation environment, lithography, process, and device simulation steps are coupled very tightly. For example, process and device steps are performed for each CD value, even if it is numerically indistinguishable from a previously evaluated one. In the future, exiguous CD variations should not lead to repeated computations. In addition to the physical gate length, other device parameters such as the shallow trench isolations (STI), should be obtained by lithography simulation. Furthermore, topography effects, for example, as induced by etching steps, could be taken into account. Future work will also aim at a coupled lithography/device process optimization using both lithography and device related figures of merit.

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